between the pixel electrode and the common electrode, the electric field generated between the surrounding wiring and the pixel electrode is hard to be effused into the liquid crystal layer, so that the bend-type orientation is hard to disturb. In order to arrange the pixel electrode at a closer position to the common electrode than the positions of the signal and scanning lines to the common electrode, an insulating layer is formed between the signal and scanning lines and the pixel electrode.

**On page 7, please delete the third full paragraph and replace it with the following new paragraph:**

The electric field generated between the pixel electrode and the signal and 15 scanning lines is generated mainly from an origin located at respective end portions. Accordingly, if the end portions of the pixel electrode overlap through an insulating layer with the end portions of the signal and scanning lines, since the electric field generated between the pixel electrode and the signal and scanning lines is generated at the rear side of the pixel electrode, the effect of the vertical electric field is further reduced.

**On page 9, please delete the first full paragraph and replace it with the following new paragraph:**

The tilt angle of the liquid crystal molecules is liable to be affected by irregularities of the substrate surface. That is, if the substrate surface is inclined in the direction opposite to the tilt angle, the liquid crystal molecules will be oriented in undesirable directions, which may disturb the normal bend-type orientation of the liquid crystal molecules. If irregularities of the opposing surface of the active matrix substrate, formed by repeated lamination and etching, can be

eliminated and a flat and smooth surface is obtained, tilting of the liquid crystal molecules in the undesirable direction can be prevented and the normal bend-type orientation can be obtained. The flat and smooth surface can be provided by formation of a thick organic insulating film.

**On page 14, please delete the second full paragraph and replace it with the following new paragraph:**

A chromium film having a thickness of 0.2 μ m is formed on a substrate 1 by a sputtering method, and scanning lines 11 and gate electrodes 12 are formed by patterning the chromium film by photolithography. It is noted that, although the chromium is described as above, the other metal materials, having low electric resistivities and which can be patterned by photolithography, such as molybdenum, titanium, aluminum, aluminum alloys may be used. In addition, the scanning lines 11 and the gate electrode 12 may be formed not only by the chromium film but also by the composite film laminated with a barrier metal of titanium on the chromium film. Subsequently, a silicon nitride film with a thickness of 0.5 μ m is formed as the gate insulating layer 2 by chemical vapor deposition (hereinafter, called CVD). On the gate insulating layer 2, an undoped A-Si layer and n+ type a-Si are formed by CVD for forming an a-Si film 15 by patterning these CVD films. Here, the a-Si film is used as an active layer of the transistor, and the n+ type a-Si is used for ensuring ohmic contact between the drain electrode 32 and the source electrode 33.

**On page 14, please delete the third full paragraph and replace it with the following new paragraph:**

Subsequently, contact holes for electrically connecting the signal lines, the source electrode, and the drain electrode with the conductive layer for forming the pixel electrodes are formed by patterning the gate insulating layer 2. It may not be necessary to form contact holes. It may be possible to provide conductivity in ways other than the use of contact holes. Subsequently, a chromium film with a thickness of 0.2 μ m is formed on the a-Si film 15 and the n+ type a-Si 16 and the signal lines 31, the drain electrode, and the source electrode are formed by sputtering the chromium film. Although the chromium film is used for forming the signal lines, it is possible, as for the scanning lines, to use other metals such as molybdenum, titanium, aluminum, and aluminum alloy, when the metals have low resistivity and can be patterned by photolithography. In addition, the scanning lines 11 and the gate electrode 12 may be formed not only by the chromium film but also by a composite film laminated with a baffler metal of titanium on the chromium film.

**On page 17, please delete the first full paragraph and replace it with the following new paragraph:**

Further, a potential difference is generated between the signal lines 31 and the pixel electrode 41, which is a parasitic potential which is not originally desired. Since the signal lines 31 and the pixel electrodes 41 are arranged horizontally on the same layer, the electric field Ef2 generated by this potential difference is a horizontal electric field, and the directions of the force lines coincide with the short side axis A-A', that is, the orientation direction Or of the liquid crystal molecules. Accordingly, this horizontal electric field Ef2 does not change the liquid crystal molecules into a twisted orientation before the liquid crystal molecules change to the

bend-type application mode. Thus, by arranging the orientation directions Or of both substrates facing each other to tend toward the short side axis A-A7, the effect of the horizontal electric field on the liquid crystal molecules can be avoided. A similar effect can be obtained when the liquid crystal is oriented in the inverted direction by rotating 180 degrees. Practically, this effect can be realized when the orientation tends toward a direction within ± 45 degrees of the short side of the pixel region. Accordingly, a parasitic horizontal electric field is generated between the scanning lines and the pixel electrodes. However, since the length of each scanning line facing the pixel electrode is small (that is, since the scanning lines face to the pixel electrode in the direction of the short side axis), the effect of the parasitic electric field is small. In addition, in this constitution, which is described later, since the scanning lines are formed in a lower layer than the layer of the pixel electrode, the parasitic electric field will not penetrate too much into the cell gap.

**On page 19, please delete the first full paragraph and replace it with the following new paragraph:**

Similar to the first embodiment, the scanning lines 3 and the gate electrode 12 are formed by forming a chromium film with a thickness of 0.2 μ m and by patterning by the photolithographic technique. Then, the silicon nitride film for forming the gate insulating layer 2 is deposited at a thickness of 0.5 μm. On the gate insulating layer 2, an undoped a-Si and an n+-type a-Si layer are deposited by CVD, and by patterning these layers, the a-Si layers 15 are formed. Subsequently, contact holes are formed by patterning the gate insulating layer 2 in order to conductively connect the conductive layer including the scanning lines 11 and the conductive

layer including the signal lines, the source electrodes, and drain electrodes, which are formed in a later process. These contact holes are formed when they are necessary. The conduction may be obtained by other methods. Subsequently, a chromium film with a thickness of 0.2 μ m is formed by sputtering on the a-Si layer 15 and the n+ -type a-Si layer and, by patterning, the signal lines 31, drain electrodes 32, and source electrodes 33 are formed. Subsequently, dry etching is executed using a gas, which is capable of etching the n+-type a-Si, for removing the n+ -type a-Si layer located between the drain electrodes 32 and the source electrodes 33. Subsequently, the silicon nitride film is formed by CVD with a thickness of 0.2 μ m for forming the intermediate insulating layer 9. The intermediate insulating layer 9 not only functions as the intermediate layer between the layer including the pixel electrodes and the layer including signal lines etc., but also functions as a protective insulating layer 3 as described in the first embodiment for preventing impurity ions from penetrating in the a-Si layer and prevents the thin film transistors from causing a malfunction. Subsequently, the orientation film made of polyimide resin is formed by a printing method, and after firing at 220°C, the orientation film is orientation treated in the short side direction by a rubbing process.

**On page 23, please delete the fourth full paragraph and replace it with the following new paragraph:**

The same processes as those of the second embodiment are followed until forming the pixel electrode 41, and the n+-type a-Si film located between the drain electrode and the source electrode is removed. Subsequently, a flat protective insulating layer is formed by spin coating an acryl-base transparent resist into a thickness from 1 μ m to 4 μ m and by firing the coat. In

Q8 Cont.

this manufacturing process, an acryl base resist has been used, but it is possible to use other resists. For example, polyimide-type resists can be used if a flat surface is obtained. It is preferable to use benzocyclobutene or polysilazane containing silicone in the coatable state in order to improve the protective function of the a-Si layer. It is also possible to use silicon nitride film before coating the acryl-type resist film.

**On page 24, please delete the first full paragraph and replace it with the following new paragraph:**

Q9

In addition to forming the flat surface by coating the resin film, it is also possible to form an insulating layer by CVD or sputtering, and to grind the surfaces of films for finishing to flat films. A very flat surface obtained by grinding the insulating film deposited by CVD or sputtering allows high precision patterning, and the thus formed insulating film provides a layer with high thermal resistance.

**IN THE CLAIMS:**

**Please cancel claims 10-11 without prejudice or disclaimer.**

**Please enter the following amended claims:**

Q10

8. (Amended) An OCB-type liquid crystal display device according to claim 6, wherein said compensation electrode is formed so as to connect to the scanning line of the adjacent pixel region.